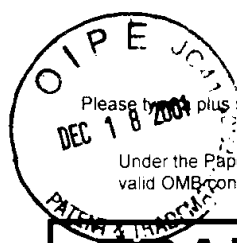


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PTO/SB/21 (12/97)  
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<b>TRANSMITTAL FORM</b> (to be used for all correspondence after initial filing)	Application Number	09/731,596
	Filing Date	December-06, 2000
	First Named Inventor	Margaret Fyfield
	Group Art Unit	2825
	Examiner Name	Kik, P.
	Attorney Docket Number	100.365 / 00-103
Total number of pages in this submission		5

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Individual Name	Sandeep Jaggi, Reg. No. 43,331, Phone: [+1] 408-433-7191
Signature	
Date	12-12-00

CERTIFICATE OF MAILING	
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope to: Assistant Commissioner for Patents, Washington, D.C. 20231 on this date: 12/13/01	
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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Margaret Fyfield

Serial No.:

09/731,596

Filed:

December 06, 2000

For:

Probing Fixture And Method For  
Semiconductor Wafer



Group Art Un

2825

Examiner:

Kik, P.

Atty Docket:

100.365 / 00-103

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Connie Del Castillo

12/13/01 *Connie Del Castillo*

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Signature

## CERTIFICATION UNDER 37 C.F.R. 3.73(b)

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

LSI Logic Corporation, a Delaware corporation, certifies that it is the assignee of the entire right, title and interest in the patent application.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of the undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

LSI Logic Corporation  
1551 McCarthy Blvd., MS D-106  
Milipitas, CA 95035  
(408) 433-8708

Date: 12/12/01

Respectfully submitted,

*Sandeep Jaggi*  
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Chief IP Counsel  
Corporate Assistant Secretary  
LSI LOGIC CORPORATION